Remarks

Upon entry of the foregoing amendment, claims 17-33 are pending in the application, with 17, 24, 28, 32, and 33 being the independent claims. Claims 17, 24, 28, 32, and 33 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 17-20, 24, and 25 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,317,820 to Shiell et al. (hereinafter "Shiell"). Applicant respectfully traverses this rejection. Independent claim 17, as amended, recites:

> A system to process very long instruction words (VLIWs), the system comprising:
>
> *a decode unit to decode an instruction of a VLIW received during an instruction fetch*, wherein all instructions of the VLIW have the same predetermined instruction bit length; and
>
> first and second processing channels, each processing channel including a plurality of functional units, at least one of the functional units of each processing channel being a data processing unit and at least one other of the functional units of each processing channel being a memory access unit;
>
> wherein the decode unit is *operable to determine whether the instruction defines a single operation or two independent operations and to control the first and second processing channels based on the determination.*

On page 9 of the Office Action, Examiner relies on col. 3, lines 60-67 of Shiell to allegedly show that Shiell teaches an instruction within an instruction sequence that includes more than one operation. Specifically, Examiner asserts that VLIW instructions have multiple operations. Applicant agrees that a VLIW can have multiple instructions.

In fact, independent claim 17, as amended, calls for all instructions of the VLIW to have the same predetermined instruction bit length. However, nothing in the cited material suggests that an instruction of the VLIW received during an instruction fetch can define *a single operation or two independent operations.*

On page 3 of the Office Action, Examiner relies on col. 2, lines 23-56 of Shiell to allegedly show a decode unit that is operable to determine whether the instruction defines a single operation or two independent operations. However, the cited art merely describes which data registers and functional units execute instructions, depending on the mode.

Nothing in the cited material suggests a decode unit that is *operable to determine whether the instruction* (of the VLIW received during the instruction fetch) *defines a single operation or two independent operations...*, as set forth in independent claim 17, as amended.

Independent claim 24 also distinguishes over Shiell for reasons similar to those set forth above with respect to independent claim 17, as amended, and further in view of its own features. Furthermore, claims 18-23, which depend from claim 17, and claims 25-27, which depend from claim 24, are also patentable over Shiell for at least these reasons, and further in view of their own features. Therefore, Applicant respectfully requests that the § 102 rejections be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

Claims 21-23, 26, 27, and 32 were rejected under 35 U.S.C. § 103(a) as being obvious over Shiell in view of U.S. Patent No. 5,761,470 to Yoshida (hereinafter

"Yoshida"). Applicant respectfully traverses this rejection. Independent claim 32, as amended, recites:

> A method of operating a system that processes very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, the method comprising:
>
> fetching the VLIW from a program memory;
>
> *decoding each instruction of the VLIW, wherein decoding each instruction includes reading the identification bit of each instruction to determine*:
>
> a) *whether the instruction defines a single operation or two independent operations*, and
>
> b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.

Claim 32 distinguishes over Shiell for reasons similar to those set forth above with respect to independent claim 17, as amended, and further in view of its own features. More specifically, Shiell and/or Yoshida, alone or in combination, fail to teach or suggest *decoding each instruction of the VLIW, wherein decoding each instruction includes reading the identification bit of each instruction to determine whether the instruction defines a single operation or two independent operations.*

Claims 21-23, 26, and 27 are also patentable over Shiell and Yoshida, alone or in combination, for at least these reasons, and further in view of their own features.

Claim 28 was rejected under 35 U.S.C. § 103(a) as being obvious over Shiell in view of U.S. Patent No. 6,697,774 to Panesar (hereinafter "Panesar"). Applicant respectfully traverses this rejection. Independent claim 28, as amended, recites:

> An article comprising a medium for storing commands to enable a processor-based system to:
>
> process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length, wherein *the commands to enable the processor-based system to process the very long instruction word data include commands to*

enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations;

when the instruction defines two independent operations, supply one of the independent operations to a first processing channel and supply the other of the independent operations to a second processing channel, wherein the two independent operations are executed simultaneously; and

when the instruction defines a single operation, control the first and second processing channels to cooperate to execute the single operation.

Claim 28 distinguishes over Shiell for reasons similar to those set forth above with respect to independent claim 17, as amended, and further in view of its own features. More specifically, Shiell fails to teach or suggest that *the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations.*

Panesar describes a modelling tool for use in defining an application specific processor (ASP). Panesar has nothing to do with determining whether an instruction of a VLIW defines a single operation or two independent operations. Thus, Panesar fails to remedy the failure of Shiell to teach or suggest that *the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations.*

Claims 29-31 and 33 were rejected under 35 U.S.C. § 103(a) as being obvious over Shiell in view of Yoshida and Panesar. Applicant respectfully traverses this rejection. Independent claim 33, as amended, recites:

> An article comprising a medium for storing commands to enable a processor-based system to:
>
> process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, wherein *the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine:*
>
> a) *whether the instruction defines a single operation or two independent operations*, and
>
> b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.

Claim 33 distinguishes over Shiell, Yoshida, and Panesar for reasons similar to those set forth above with respect to independent claims 17, 28, and 32, all as amended, and further in view of its own features.

Claims 29-31 are also patentable over Shiell, Yoshida, and Panesar, alone or in combination, for at least these reasons, and further in view of their own features.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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